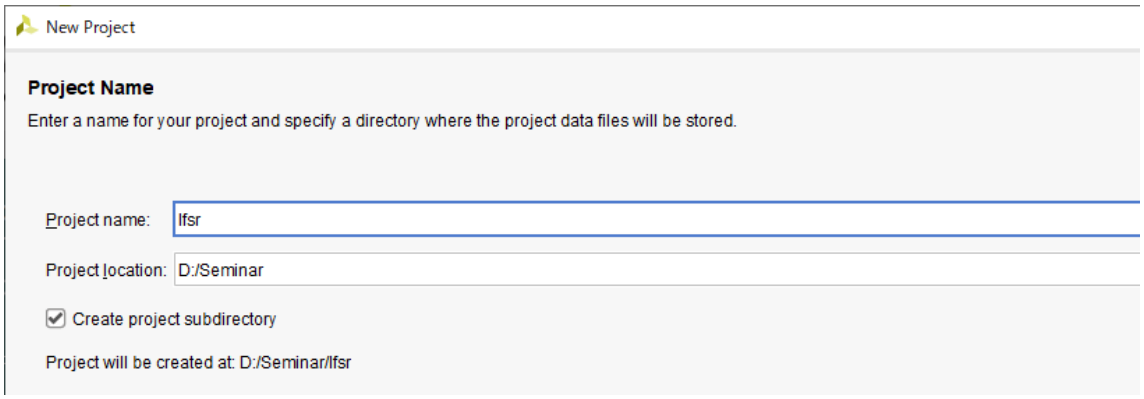
Vivado Simulator and Testbench

Introduction

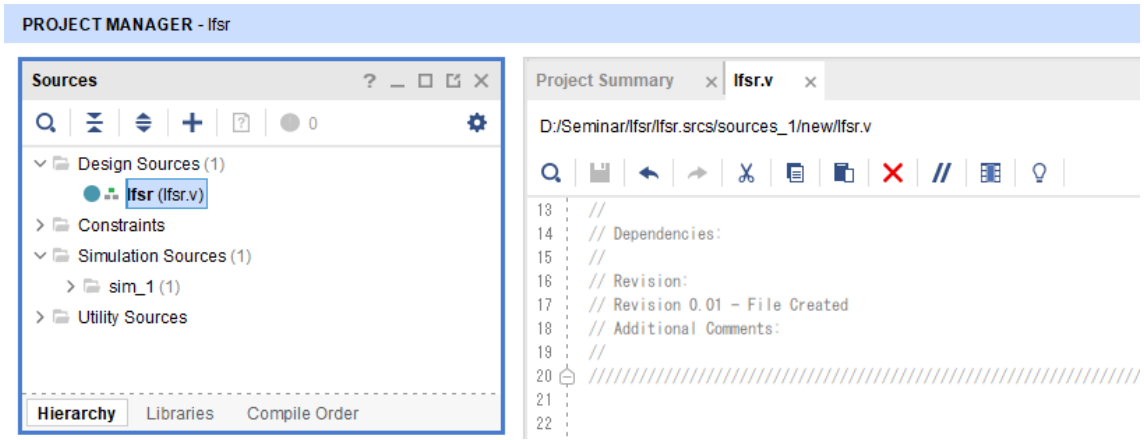
This tutorial walks through a simple demonstration of how to develop your testbench using Vivado's behavioral simulation. Vivado's behavioral simulation runs a specified testbench module and displays the logic of the testbench's results in a waveform window. This allows a developer to verify the proper functionality of every RTL module in a design at any time without needing to run synthesis or implementation.

1. Creating RTL Module

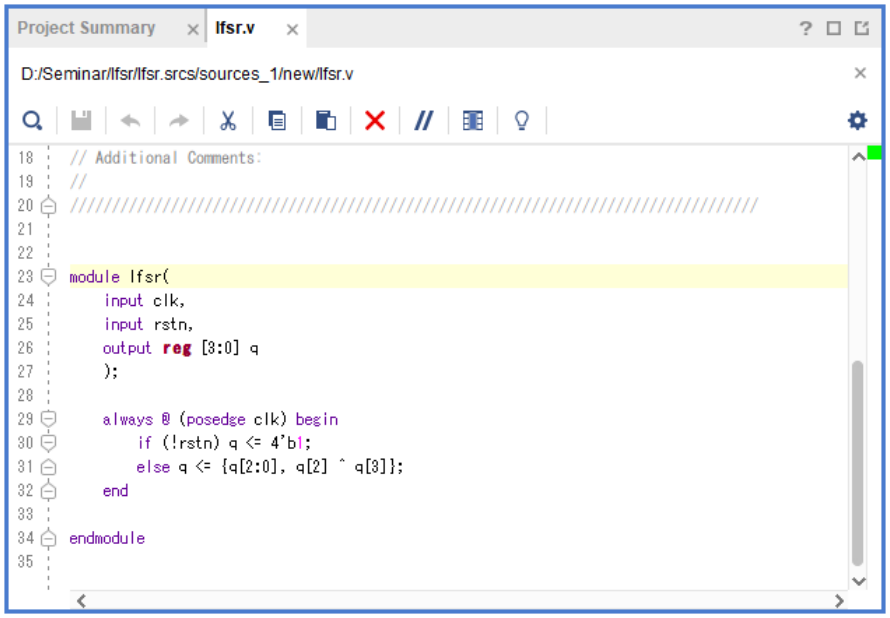
1.1) Create **lfsr** project.



1.2) Create **lfsr.v** design source to the project.

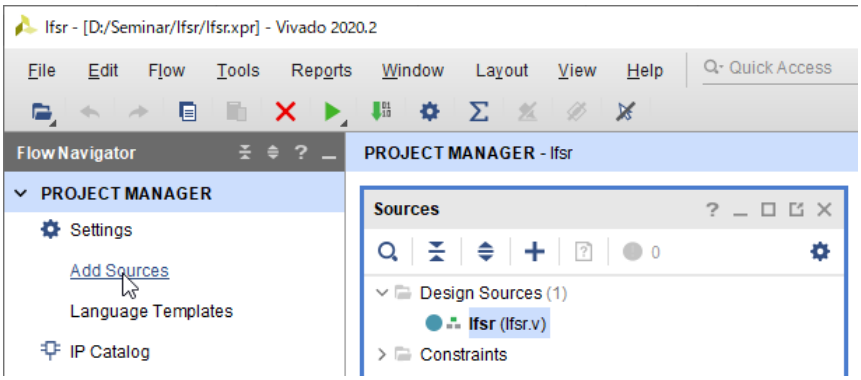


1.3) Write the 4-bit linear feedback shift register Verilog code into the text editor.

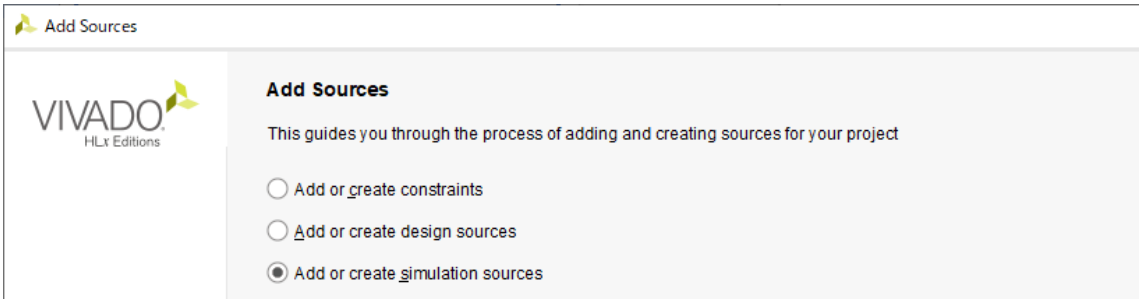


2. Creating Testbench Module

2.1) Click **Add Sources** in the "Flow Navigator".

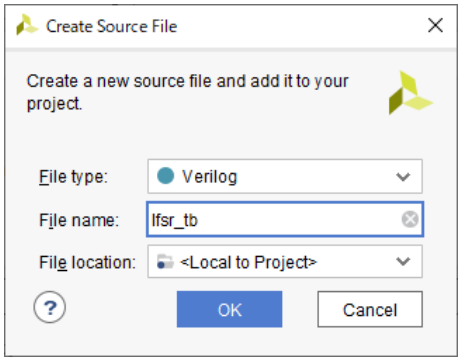


2.2) In the "Add Sources" form, select **Add or create simulation sources**. Click **Next**.

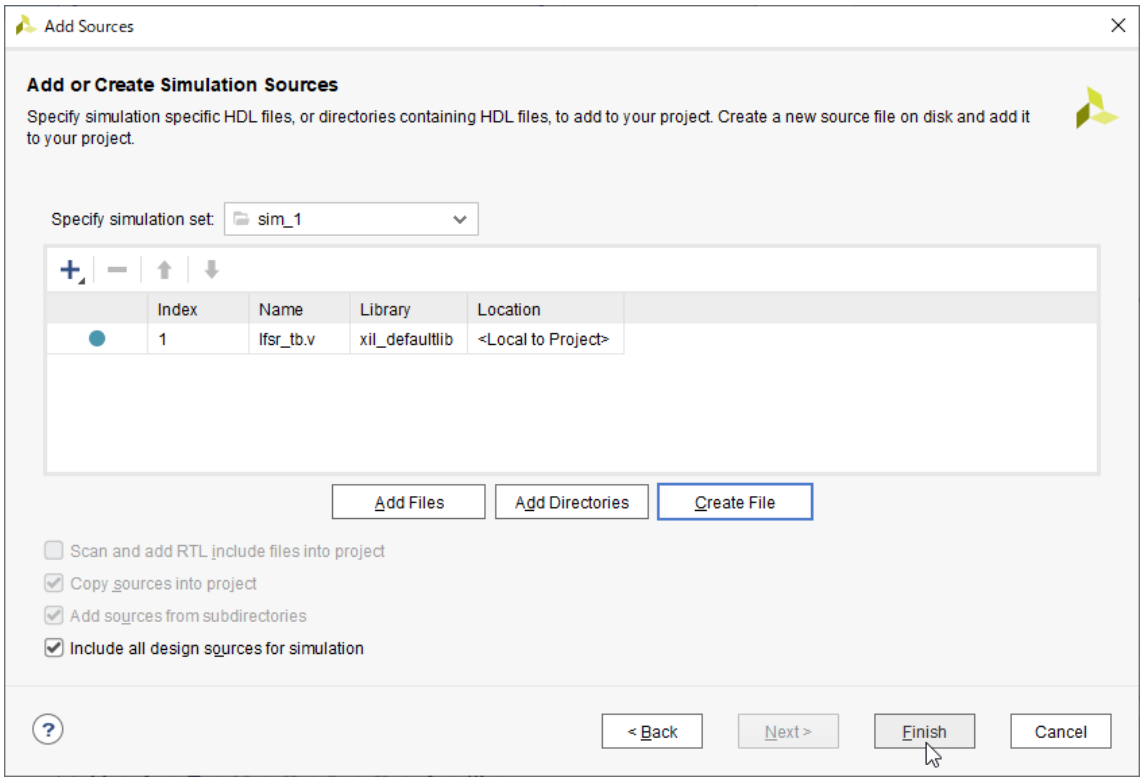


2.3) In the "Add or Create Simulation Sources" form, click **Create File** button.

2.4) In the “Create Source File” form, select **Verilog** in the “File type” field. Enter **lfsr_tb** in the “File name” field. Click **OK**.



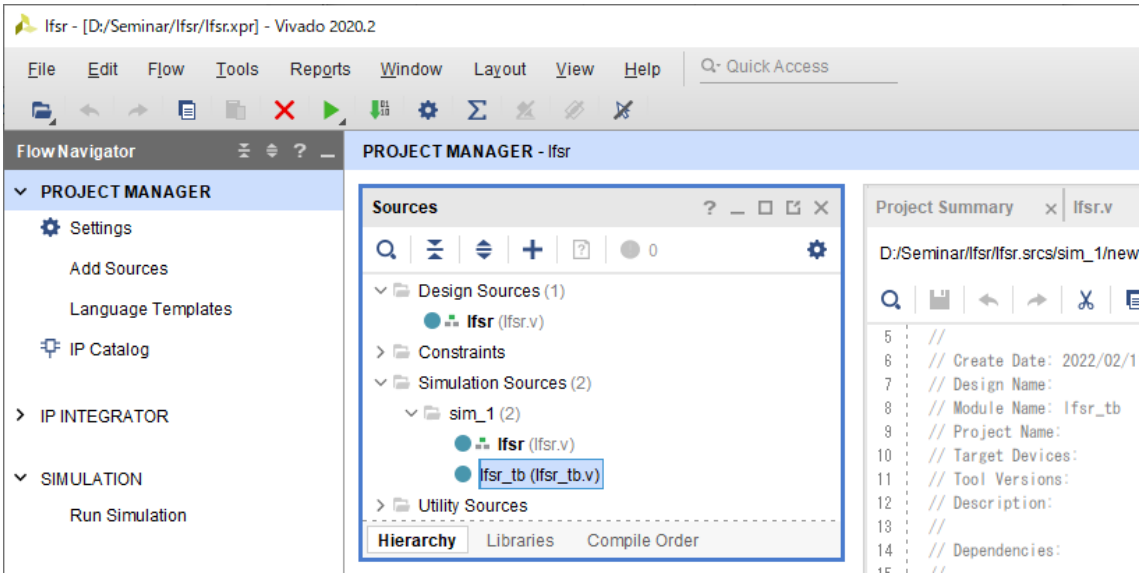
2.5) You will see the created file in the “Add or Create Simulation Sources” form. Click **Finish**.



2.6) Skip the “Module Definition” form by clicking **OK**.

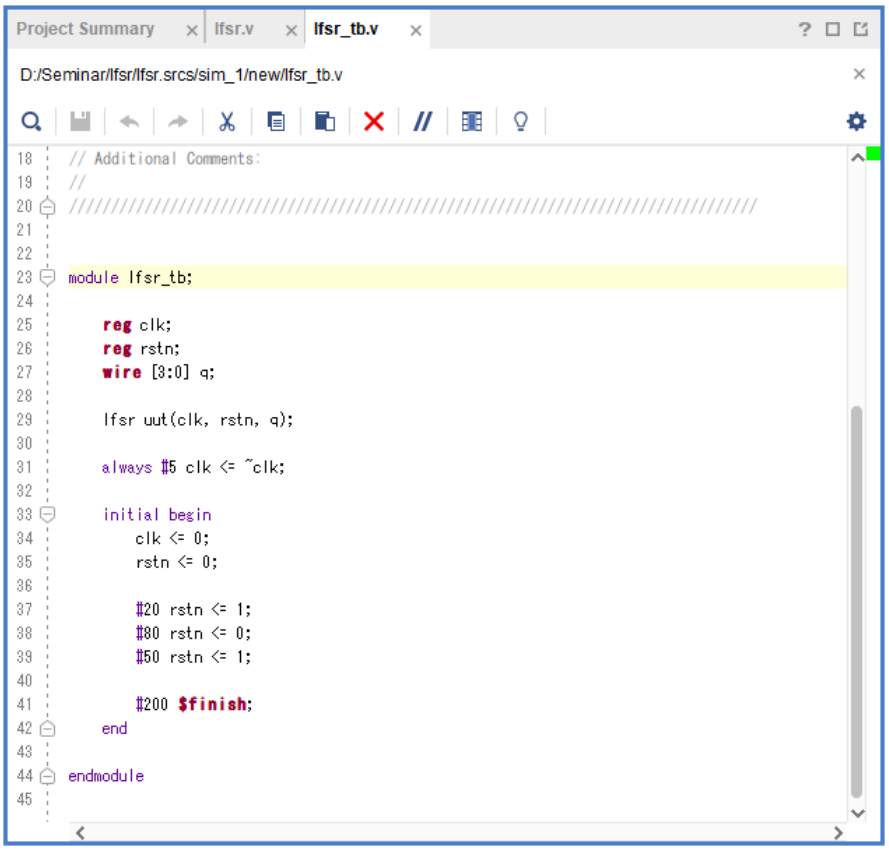
2.7) You will see the “Define Module” dialog box. Click **Yes**.

2.8) The created file will be added to the “Simulation Sources” folder in the “Sources” pane of the “PROJECT MANAGER”.



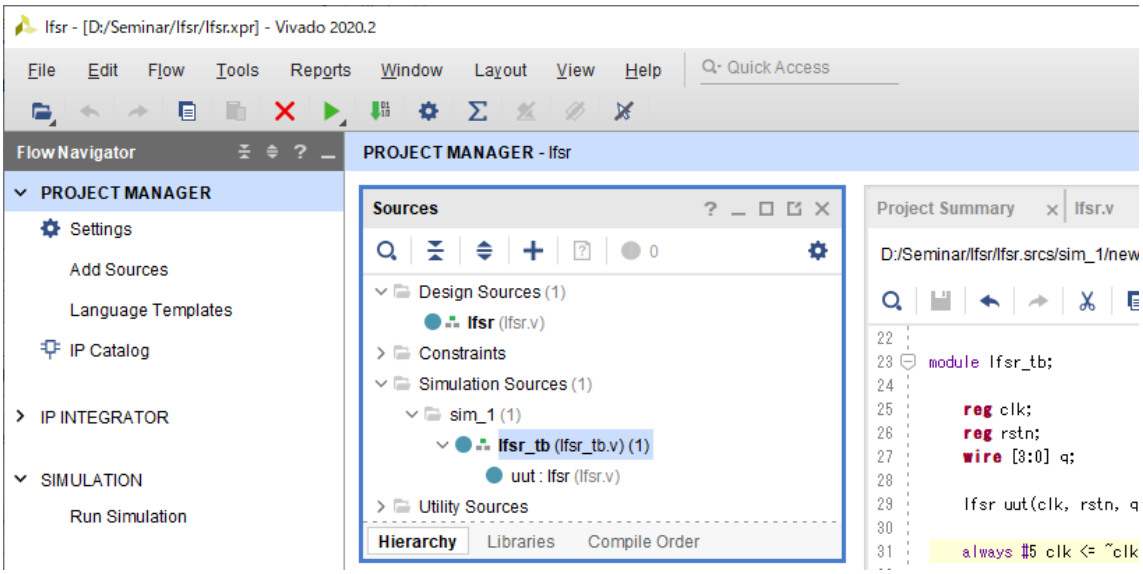
2.9) Double click on the **lfst_tb.v** file in the “Sources” pane to open it.

2.10) Write the testbench code into the text editor.



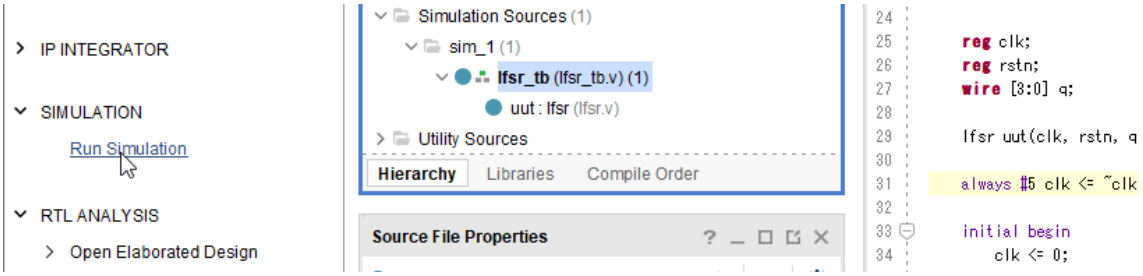
2.11) Ctrl + S to save the file.

2.12) Vivado automatically updates the hierarchy of the modules and instances and set the testbench as the top module of the project.

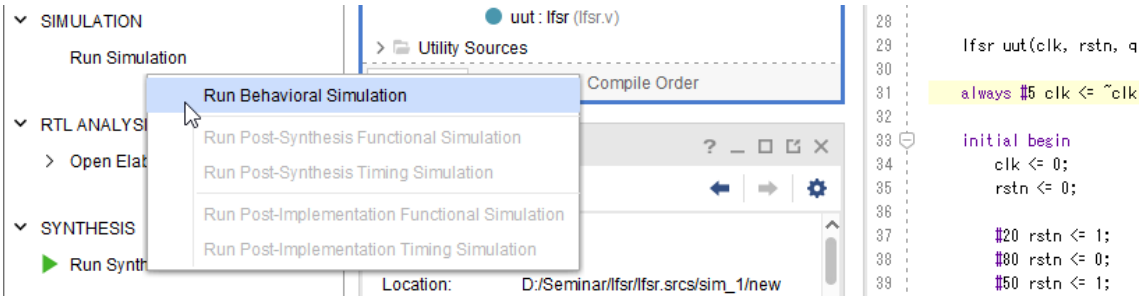


3. Running Behavioral Simulation

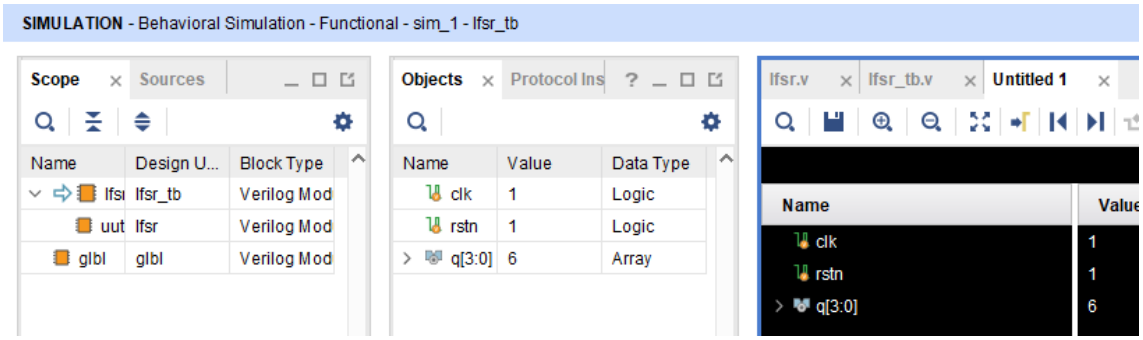
3.1) Click **Run Simulation** in the “Flow Navigator”.



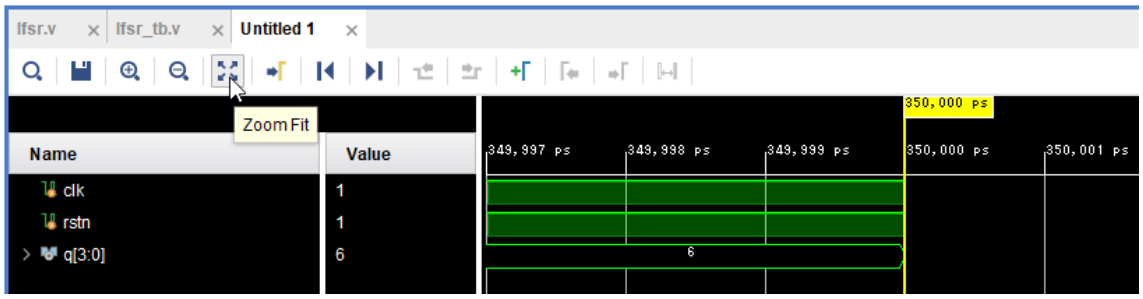
3.2) Select **Run Behavioral Simulation**.



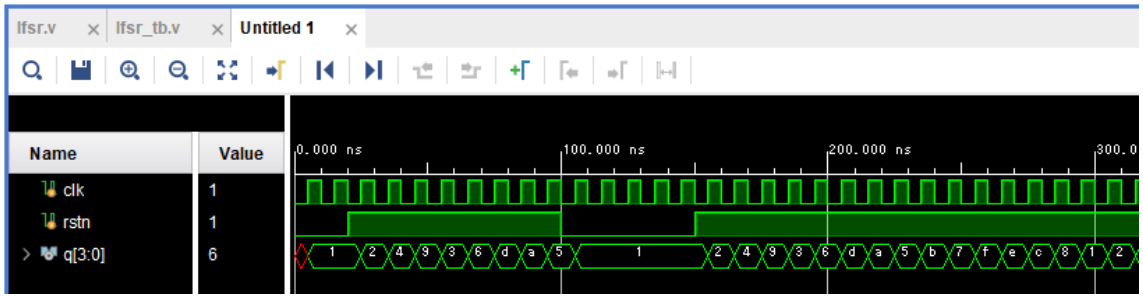
3.3) The “SIMULATION” pane opens after successfully completing the simulation process.



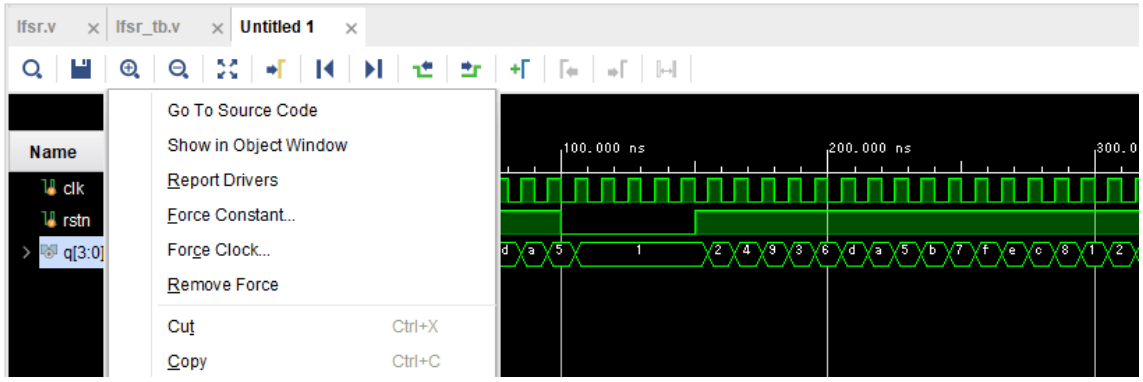
3.4) Click **Zoom Fit** icon in the waveform window.



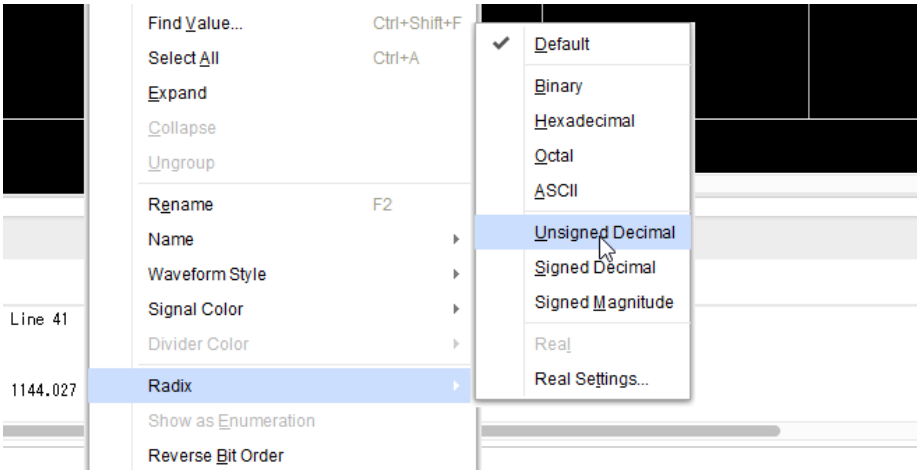
3.5) Now you can see the entire waveform.



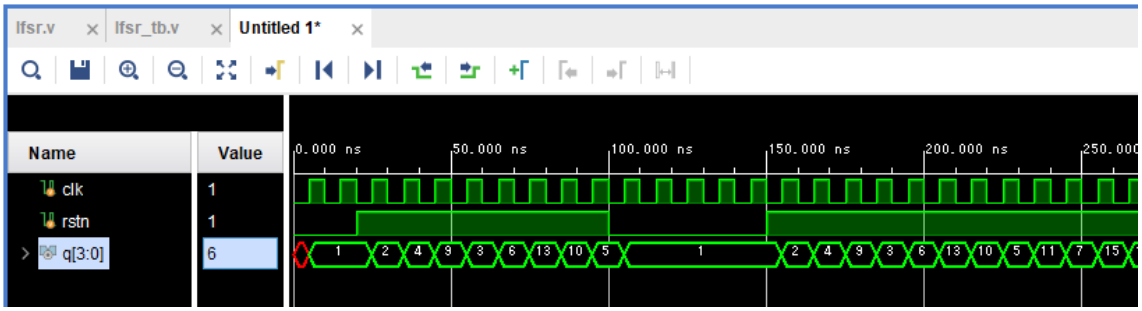
3.6) In the waveform window, select **q[3:0]** signal and right click to open popup menu.



3.7) From the popup menu, select **Radix > Unsigned Decimal**.

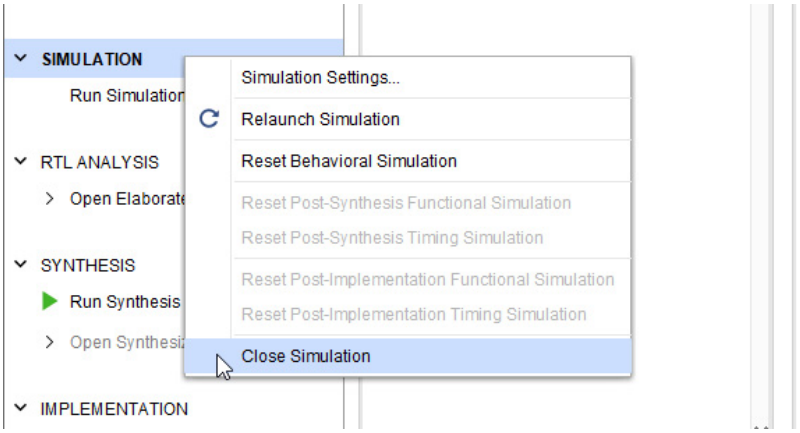


3.8) The values in the waveform are shown in decimal.



4. Closing Simulation

4.1) Click **Run Simulation** in the "Flow Navigator" and select **Close Simulation**.



4.2) You will see the "Confirm Close" dialogue. Click **OK**.